REMARKS

This is a response to the Office Action dated September 8, 2004, in which oath and declaration were objected to as being defective, specification was objected to because of several informalities, and claims were objected to under 35 U.S.C. § 112 ¶¶ 1 and 2. Individual issues raised by the Examiner in the Office Action will be addressed next.

Objection to the Oath or Declaration

In paragraph 3 of the Office Action, the declaration of the application was objected to as being defective. In response, applicant respectfully submits that the declaration executed on February 12, 2002 is not defective as it properly establishes inventorship of the present application. In particular, Seong Yong Kim is the sole inventor as indicated in the executed declaration filed on February 12, 2002, while Sung Hun Park was mistakenly added to the unexecuted declaration submitted on October 25, 2001. Accordingly, the unexecuted declaration of October 25, 2001 should be discarded and the declaration of February 12, 2002 executed by Seong Yong Kim should be admitted into the present case. Applicant believes that a new declaration is not required here because February 12, 2002 declaration was properly executed by Seong Yong Kim and neither of the declarations was executed by Sung Hun Park. Furthermore, applicant believes that the assignment of the present application by the Seong Yong Kim to Inode Technologies, Inc., dated January 28, 2002 and recorded in the U.S. Patent and Trademark Office on February 12, 2002 on Reel 012596, Frame 0300, serves as a sufficient written consent of assignee for the purpose of MPEP 201.03(d).

Objection to the Specification

In paragraph 4 of the Office Action, the disclosure was objected to as containing certain informalities. Furthermore, in paragraph 5, the specification was objected to as having improper idiomatic English.

In response, applicants submits herewith a Substitute Specification in proper idiomatic English and in which all identified informalities have been corrected. The Substitute Specification contains no new mater and is believed to comply with all statutory requirements. Accordingly, applicant respectfully requests to enter the Substitute Specification in the record of the present application.

Rejection of Claims Under 35 U.S.C. 112, ¶¶ 1 and 2

In paragraphs 7 through 10 of the Office Action, the Examiner has rejected claim 1 as containing limitations not supported by the specification and claims 1-11 as being indefinite. In response, applicant canceled claim 11 and amended claims 1-10 to particularly point out and distinctly claim the subject matter which protection is being sought. Accordingly, the Examiner is respectfully requested to withdraw Section 112 rejections.

New Claims

Furthermore, applicant added new claims 12 and 13 to particularly point out and distinctly claim the subject matter which applicant regards as the invention. New claims do not contain new matter and are supported by the specification. Accordingly, the Examiner is respectfully requested to enter new claims into the record of the present application.

Submission of Certified Priority Document

In compliance with 35 U.S.C. 119(b), applicant submits herewith a Certified Copy of Korean Patent Application No. 2000-63039 filed on October 25, 2000, to which priority of the present application is claimed.

Conclusion

On the basis of the above, it is respectfully submitted that the present application is in a condition for allowance. A prompt action by the Examiner to this effect is respectfully requested. Should the Examiner have any questions or comments concerning this submission, or any aspect of the application, the Examiner is invited to call the undersigned at the phone number listed below.

Respectfully submitted,

Date: January 10, 2005

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SUBSTITUTE SPECIFICATION

MARKED-UP VERSION

ADDRESSING SYSTEM FOR USE IN STORAGE DEVICES

FIELD OF THE INVENTION

The present invention relates to an auxiliary storage device and, in particular, to a high-capacity auxiliary memory unit constructed with a memory such as SDRAM **(synchronous dynamic random access memory)** and a SCSI (small computer system interface) bus structure.

BACKGROUND OF THE INVENTION

As personal computers are widely used, a client and server system based on the personal computers now can handle tasks that were once possibly executed by a main frame computer system. Typically, a client and server system includes a high-speed server with a large-capacity auxiliary memory unit and a plurality of personal computers (clients). The server and personal computers are connected via a network, thereby allowing the clients to access the server. Specifically, each client has the ability to write and read information to and from the server and to exchange information with other clients connected to the network.

However, an increased number of clients create a bottleneck between a server and auxiliary memory units. As a result, access time would be longer and, worst, due to excessive load on the network, the network could be down or transmitted data could be lost.

In the client and server system, a hard disk drive (HDD) is dominantly used as an auxiliary memory unit. As is well known, the HDD is a large data storage device using magnetic disks. Data is stored to and read from a spinning disk by controllably positioning the read/write head over the disk. Thus, a reading/writing operation on the HDD requires a physical rotation of a motor and the lateral movement of the read/write head. In a server system such as game servers where tens of thousands of clients could simultaneously connect at one time, read and write requests from individual clients in the server can impose a serious

load to the system. Servers with the HDD having a finite access time would not be able to handle ever increasing and faster data traffic. It could adversely affect the stabilization of the servers.

In a typical HDD, there is so-called access time, a time required to seek and change discs until a head is positioned over a sector. A drive motor is rotated to move the head over the sector where data is magnetically written and read. As is well known, while a high-performance SCSI bus provides a transmission rate of 320 Mega-bytes at the maximum, the HDD provides a transmission rate of 43 Mega-bytes at the maximum due to the aforementioned problems.

CPUs used in typical servers can address only ~~**upto**~~ **up to** several Giga-byte memory map ranges so that they cannot directly control a data storage capacity over tens of Giga-bytes reaching several Tera-bytes. Furthermore, the CPUs fail directly to drive a plurality of memories due to a fan-out between memory chips.

SUMMARY OF THE INVENTION

It is, therefore, a primary objective of the present invention to provide a system, which is capable of dividing a memory into a plurality of equally-sized sub-memories and controlling an address of each sub-memory, thereby significantly increasing the access speed to an auxiliary memory unit.

In accordance with a preferred embodiment of the present invention, there is provided a system for addressing a data storage unit used in at least one of server and client computers, which comprises: ~~**means**~~ **a converting unit** for converting **a format of data on** an external bus ~~**into**~~ **so that the data are accessed on** an internal bus for use in the system; a memory **card** module **connected to the internal bus** for storing data on the internal bus ~~**therein**~~, the memory **card** module ~~**being divided into**~~ **includes a plurality of memory modules, each having** a plurality of equally-sized memory blocks; and ~~**means**~~ **a processing unit** for ~~**processing**~~ writing data on the internal bus ~~**in**~~ **to** the memory module and reading out the data

therefrom.

BRIEF DESCRIPTIONS OF THE DRAWINGS

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

FIG. 1a schematic diagram of a memory addressing system in accordance with a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram of the PCI-to-memory controller shown in FIG. 1 in accordance with a preferred embodiment of the present invention;

FIG. 3 is a detailed block diagram of the PCI interface controlling unit shown in FIG. 2 in accordance with a preferred embodiment of the present invention; and

FIG. 4 is a schematic diagram of an expanded memory addressing system 200 in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

~~**In accordance with the present invention, a data seek time is removed by converting data position information in the HDD into a corresponding memory address so that a data access time is minimized to the order of several nano-seconds. Furthermore, the present invention employs a PCI 66 MHz/64 bit bus to access internal memories, thereby supporting a transmission rate of 528 Mbytes/second at maximum, which, in turn, meets the maximum transmission rate as mentioned above. As a result, Access speed to auxiliary memory unit is at least 12 times faster than that to the conventional HDD.**~~

Referring to FIG. 1, there is shown a schematic diagram of a memory addressing system in accordance with a preferred embodiment of the present invention. The memory

addressing system 100 comprises a SCSI interface controller 10, a memory card module 20, a CPU module 30, a PCI interface bus 40, and a control signal bus 50. The SCSI interface controller 10 converts **a format of data on** an external SCSI (small computer system interface) bus ~~**into**~~ **so that the data are accessed on** an internal PCI bus adapted to the memory addressing system 100, thereby allowing a SCSI bus command to be processed by the CPU module 30. As is well known, SCSI is one of the industry's standard interfaces that allows personal computers to communicate with peripheral devices, such as disk drives, tape drives, CD-ROM **(compact disk-read only memory)** drives, printers, and scanners, faster and more flexibly than previous interfaces. SCSI ports are built into most personal computers today and supported by all major operating systems. SCSI is more flexible than earlier parallel data transfer interfaces.

The CPU module 30 controls all components of the SCSI interface controller 10, manages the internal PCI bus, and converts **information of** a head, sector and cylinder representing position information of the HDD, and **information of** a track, sector and cluster representing format information of the HDD, which are inputted through the SCSI bus, into ~~**a**~~ corresponding memory addresses.

The memory card module 20, which is composed of SDRAM, Rambus DRAM, DDR or other equivalent memories, includes a **PCI-to-memory controller** 21 and a plurality of memory modules (e.g., 22)**.** ~~**each of which has four equally-sized sub-memories**~~ **Each of memory modules 22 has a plurality of memory blocks, and each memory block has four equally-sized sub-memories**.

The PCI interface bus 40 and the control signal bus 50 are internal local buses for ~~**processing**~~ **transmitting** internal data and control signals and use the standard PCI 64-bit bus interface.

In accordance with the present invention, the memory ~~**card**~~ module ~~**20**~~ **22** ~~**is of**~~ **has** a hierarchical **memory** configuration, which includes ~~**the PCI interface controlling unit and**~~ **the plurality of memory blocks, each memory block having** a multiplicity of sub-memories, to prevent the fan-out problem. The fan-out problem occurs when signals

outputted from an original signal line are divided onto a number of lines for transmission, resulting in a decreased signal voltage. **In a high-capacity memory, the division of signals from the original signal lines is increased so that signals to be directed to each memory are eventually attenuated.**

With the tree structure of **the hierarchical memory configuration in accordance with** the present invention, signals are compensated at ~~an~~ intermediate stage**s such as the memory module and the memory block** and forwarded to lower levels **such as the sub-memories** ~~in the hierarchy~~, thereby eliminating signal loss problems. ~~In a high-capacity memory, the division of signals from the original signal lines is increased so that signals to be directed to each memory are eventually attenuated.~~ Clock delay required for **the hierarchical memory configuration to** ~~compensating~~ compensate the signals is ~~in turn~~ compensated by the memory controller 21.

Because the **PCI-to-memory controller** 21 ~~employing a tree structure~~ controls the memory module 22 distributed in a hierarchical ~~fashion~~ **memory configuration**, it can drive a physical memory that is actually accessed while ~~placing~~ the rest of **memories** maintains in a low-power mode. As a result, power used to drive the memories is reduced and a back-up batter power can be extended.

FIG. 2 is a detailed block diagram of the **PCI-to-memory controller 21** shown in FIG. 1 in accordance with a preferred embodiment of the present invention.

As shown in FIG. 2, the **PCI-to-memory controller** 21 includes a first memory controlling unit 21a, a second memory controlling unit 21b and a PCI interface controlling unit 21c. The PCI interface controlling unit 21c**, which functions as a bridge between the PCI interface bus 40 and the first and second memory controlling units 21a and 21b,** ~~processes~~ **performs** a standard PCI command, control~~,~~ **and** data **signal processing**, ~~which functions as a bridge between the PCI interface bus 40 and the first and second memory controlling units 21a and 21~~b. Each of the first and second memory controlling units 21a and 21b~~, responsive to a PCI command provided thereto from the PCI interface controlling unit 21c via a bus B2,~~ performs a direct read/write operation for ~~an internal~~ **the**

sub-memory to be accessed **in response to a PCI command provided from the PCI interface controlling unit 21c via a bus B2**, and matches information of a cylinder, head~~,~~ **and** sector~~, information in~~ **of** the HDD to ~~an~~ addresse**s of memories so as** to ~~process~~ **write** the data **to the memories**. Specifically, the first memory controlling unit 21a, responsive to the PCI command provided ~~thereto~~ from the PCI interface controlling unit 21c via the bus B2, performs a direct read/write operation for any sub-memory of the first memory module 22. The second memory controlling unit 21b, responsive to the PCI command provided ~~thereto~~ from the PCI interface controlling unit 21c via the bus B2, performs a direct read/write operation for any sub-memory of the second memory module 23. On the other side, both of the first and second memory controlling units 21a and 21b ~~process~~ **control** a high-capacity memory so that the activation of the overall memory requires a considerable amount of power consumption. As such, during the read/write operation of the memory, the first memory controlling unit 21a or the second memory controlling unit 21b activate only a memory corresponding to an address provided ~~thereto~~ from the PCI interface controlling unit 21c and maintains the remaining **memories** in a low power mode. As a result, the power consumption may be minimized.

FIG. 3 is a detailed block diagram of the PCI interface controlling unit **21c** shown in FIG. 2 in accordance with a preferred embodiment of the present invention. A detailed description of the internal operation algorithm of the PCI interface controlling unit 21c will be given with reference to FIG. 3.

As shown in FIG. 3, the PCI interface controlling unit 21c includes a configuration (CFG) register R/W 1, an I/O write 2, a memory R/W 3, and a register block 7 having a lower address bit 4, an upper address bit 5 and a select bit 6. ~~Note that, during the design of the PCI interface controlling unit 21c, from the perspective of a memory map of CPU regardless of a general-purpose or single-purpose system, the presence of an address region, which allows the CPU to address and is separated from the operation of the system, is basically required.~~ **Before designing the PCI interface controlling unit 21c, an address region, which CPU can perform addressing and is independent of operations of**

the peripheral devices, should be assigned in a memory map of CPU.

The lower address bit 4 of the register block 7 represents **an** address ~~**of a set region within the memory map, which is**~~ **included** in ~~**the range of**~~ the address region **within the memory map**. During the design of the memory controlling unit **21c**, the address range to be PCI interfaced is determined, and a bit range ~~**in which**~~ **to be used for** the lower address bit 4 ~~**is used**~~ is set, so that the lower address bit 4 is available.

The upper address bit 5 ~~**is**~~ **represents an address** set to be used when a memory address region ~~**from which**~~ **is beyond the address region in** the memory map provided by the CPU ~~**is departed**~~. In the upper memory address ~~**region**~~ **bit 5**, it is necessary to previously set a bit range based on a capacity range to be used during the design of the PCI interface controlling unit 21c.

The select bit 6 is used to directly access the memory modules and handle the fan-out to be occurred during the application of a single activation, thereby resulting in an increased **memory** expansion. From at least one bit to the maximum of the lower address ~~**region**~~ **bit 4** should be assigned to the select bit 6.

A description of the operation algorithm of the PCI interface controlling unit **21c** will be given.

During the design of the PCI interface controlling unit 21c, the lower address bit 4, the upper address bit 5 and the select bit 6 are set based on a predetermined value. The I/O write 2 sets the upper address bit 5 on the register **block 7** prior to ~~**the access to**~~ **accessing** the memory **by** using a PCI memory read/write command among the PCI commands. During the memory access, the lower address bit **4** is accessed and the lower **address** bit **4** is concatenated with an upper **address** bit **5** of the register **block 7,** which is ~~**used at**~~ **set through** the I/O ~~**interface**~~ **write 2**. Thus, the sum of the upper address bit 5 and the lower address bit 4 is used as an access memory address bit. The most significant bit of the register **block 7** is used to select any of the memory modules.

Specifically, in a CPU system with 32-bits address region for example, provided that the PCI interface controlling unit 21c is designed in conditions that ~~**from the perspective of**~~

~~the CPU~~ the lower address bit **4 depending on t CPU** is set to be 19-bits, the memory map region is set to be 1 Mbytes, the upper address bit to be I/O read and written is set to be 11-bits (i.e., 2048 bytes), and the select bit is set to be 2-bits, an available capacity of the PCI interface controlling unit may be calculated as 32 Gbytes as follows:

((1 Mbytes*2 Kbytes)*4 bytes)*4 bytes=32 Gbytes

In this manner, the application of the lower address bit, the upper address bit and the select bit to the 32-bits address region results in the capacity of 1,280,000 Tbytes. Similarly, ~~the application of them to 64-bits, 128-bits, 512-bits address region and the like results in an astronomical capacity~~ **if the address region is expanded into 64-bits, 128-bits or 512-bits address region, the memory having an astronomical capacity can be controlled**. ~~Accordingly, although a change in the system and requirements of the capacity increase in geometric progression, the present invention has the ability to easily address the change and the requirements.~~

FIG. 4 is a schematic diagram of an expanded memory addressing system 200 in accordance with another embodiment of the present invention.

As shown in FIG. 4, a plurality of PCI bridges 110~~,~~ **and** 120~~, . . . is~~ **are** used to expand the system while minimizing a change in hardware, each of the PCI bridges being provided between the PCI buses. In accordance with the present invention, although the SCSI ~~interface~~ controller is used based on Ultra-160 SCSI scheme for a data transmission between an external interface **bus** ~~via~~ the PCI **interface** bus, another data bus transmission scheme such as an IDE (Integrated Device Electronics), ATA (Advanced Technology Attachment)~~,~~ **or** IEEE (Institute of Electrical and Electronics Engineers) 1394 may be used in lieu of the SCSI.

As demonstrated above, the present invention employing ~~a tree~~ **the** hierarchical **memory** configuration, automatically activates individual SDRAM control blocks, which are not accessed in a low power mode, which, in turn, results in minimized power consumption and a low power activation.

Furthermore, in accordance with the present invention, ~~the application of a lower~~

~~address bit, an upper address bit and a select bit to various types of address regions results in an astronomical capacity, which may be controlled by CPU~~ as the address region of the lower address bit, upper address bit and the select bit is expanded into 64-bits, 128-bits, 512-bits address region, the memory having an astronomical capacity can be controlled by CPU. ~~Thus, although a change in the system and requirements of the capacity increase in geometric progression, it has the ability to easily address the change and the requirements.~~

Also, in accordance with the present invention, the memory is accessed instead of accessing the HDD. This is accomplished by converting data position information in the HDD into corresponding memory addresses so that a data access time is minimized to the order of several nano-seconds due to removal of data seek time required in the HDD. Furthermore, the present invention employs a PCI 66 MHz/64 bit bus to access internal memories, thereby supporting a transmission rate of 528 Mbytes/second at maximum, which, in turn, meets the maximum transmission rate of the high-performance SCSI bus.

While the present invention has been described and illustrated with respect to a preferred embodiment of the invention, it will be apparent to those skilled in the art that variations and modifications are possible without deviating from the broad principles and teachings of the present invention which should be limited solely by the scope of the claims appended hereto.

ABSTRACT

Please replace the abstract of the disclosure with the following text:

Disclosed is a system, which divides a memory into a plurality of equally-sized sub-memories and controls an address of each sub-memory, thereby significantly increasing the access speed to an auxiliary memory unit, which ~~comprises~~ **includes** a SCSI (Small Computer System Interface) ~~interface~~ controller for converting **a format of data on** a SCSI interface bus ~~into~~ **so that the data are accessed on** a PCI(Peripheral Component Interconnect ~~Bus~~) interface bus for use in the system, a memory card module for storing data on the PCI interface bus therein, the memory card module being divided into a plurality of equally-sized memory blocks, and a CPU (Central Processing Unit) module for ~~processing~~ writing data on the PCI interface bus ~~in~~ **to** the memory card module and reading out the data therefrom. The memory card module includes a **PCI-to-memory controller** ~~of a tree hierarchical configuration~~, which is disposed between the PCI interface bus and the plurality of ~~sub-memories~~ **the memory module having a plurality of sub-memories** as a bridge, for controlling access to the plurality of sub-memories, which is distributed in a hierarchical ~~fashion~~ **memory configuration**.